



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/415,060	10/12/1999	TAKASHI YANO	0378-0360P	4255

7590

07/31/2003

BIRCH STEWART KOLASCH & BIRCH LLP  
P O BOX 747  
FALLS CHURCH, VA 220400747

EXAMINER

TRAN, NHAN T

ART UNIT

PAPER NUMBER

2615

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/415,060

Applicant(s)

YANO, TAKASHI

Examiner

Nhan T. Tran

Art Unit

2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 October 1999.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 October 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Drawings*

The drawings are objected to because Figures 4 and 5 show "IMEGE SIGNAL" which should be changed to - IMAGE SIGNAL -. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5 – 8, 10 – 11 & 15 – 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe (US 6,529,236).

Regarding claim 1, Watanabe discloses a solid state image pickup apparatus comprising:

Art Unit: 2615

a mode setting circuit for allowing an operator to select desired one (partial pixel read mode, i.e.,  $\frac{1}{4}$  read mode) of plurality of modes (partial read mode, full pixel read mode, isochroous mode, asynchronous mode) matching with a display format of a displays a video signal fed thereto (see Figs. 1A-5; col. 4, lines 24-34 & col. 6, lines 6-23);

a clock generating circuit for generating a plurality of clocks (corresponding to plurality of modes) including a first clock (e.g., clock for driving  $\frac{1}{4}$  read pixel mode) and a second clock (e.g., clock for driving full pixel read mode) higher in frequency than the first clock (see Figs. 3 & 5; col. 4, lines 25-34. It is noted that the clock for driving the full pixel read mode in Fig. 3 must be faster than the clock for driving the  $\frac{1}{4}$  pixel read mode in Fig. 5 since the full mode requires two fields to read out all pixels for interlace while the  $\frac{1}{4}$  read mode skips reading out some pixels and reads one frame at a time which requires slower clock for reading and transferring compared to the full mode);

a frequency selector for selecting either one of a first clock and a second clock in accordance with a mode fed from the mode setting circuit (see Figs. 1A, B, 3-5 & col. 3, lines 6-10 wherein CCD drive control must select a driving clock for the CCD for each pixel read mode);

an image pickup section (22) including a plurality of photosensitive cells for transforming, by photoelectric transduction, light incident thereto from a scene to be picked up, the image pickup section picking up the scene and producing signal charges representative of the scene in accordance with an output of frequency selector (see Figs 1A, B, 3-5; col. 4, lines 4-33);

a noise reducing circuit (28) for reducing noise components included in a signal output from the image pickup section (see Fig. 1A; col. 5, lines 14-19);

Art Unit: 2615

a digitizing circuit (30) for converting an output of the noise reducing circuit to a digital signal in accordance with the first clock (see Fig. 1A; col. 5, lines 26-42 wherein the first clock is selected in accordance with selected pixel read mode);

a signal processing circuit (32) for processing an output of the digitizing circuit in a manner matching with picture display (see Fig. 1A; col. 6, lines 6-23);

a controller (CPU 26) for controlling the clock generating circuit, the frequency selector, the image pickup section, the noise reducing circuit, the digitizing circuit and the signal processing (see Figs. 1A-B wherein all processes in the camera is controlled by the Central Processing Unit 26);

wherein the plurality of modes include a first mode (i.e.,  $\frac{1}{4}$  pixel read mode) in which the frequency selector outputs the first clock (clock for driving  $\frac{1}{4}$  pixel read mode) and second mode (i.e., full pixel read mode) in which the frequency selector outputs the second clock (clock for driving full pixel read mode) (see Figs. 3-5 for the read modes of the CCD wherein each mode is driven by its corresponding clock in order for the CCD to function properly).

Regarding claim 5, Watanabe discloses vertical transfer path VCCD and horizontal transfer path HCCD in which the drive signal (100) of the first clock for driving  $\frac{1}{4}$  pixel read mode is fed to the transfer paths of the image pickup section (22). A resetting device must be included either in VCDD or HCCD or both in order for a control signal (also 100) to drive the VCCD and HCCD to reset (discharge) signal charges detected on the transfer paths after transferring mixed signals in one frame in order to receive subsequent signal charges for the next frame (see Fig. 5; col. 4, lines 55-63).

Regarding claim 6, Watanabe discloses a fourth mode (camera record mode as shown in Figs. 10 & 11) in which the output (signal 100) to be fed to the resetting device (in VCCD or HCCD) comprises the first clock (clock for driving  $\frac{1}{4}$  read mode) while an output of the frequency selector comprises the second clock (clock for driving full read mode). It is noted that the second clock is selected when the user releases command for capturing an image to a memory (14) through operation member while the first clock maintains for displaying real time images on the display (also see col. 14, line 61 – col. 15, line 31). With respect to a “third mode”, it is disclosed by Watanabe as a display mode for real time image display utilizing only the first clock of  $\frac{1}{4}$  read mode for both driving and resetting control.

Regarding claim 7, as shown in Figs. 3-5, it is clear that the clocks for driving full read mode and  $\frac{1}{4}$  read mode must be in integral ratio to each other (i.e., 4 or  $\frac{1}{4}$ ).

Regarding claim 8, Watanabe discloses VCCD and HCCD for transferring signal charges output from photosensitive device (PD) in direction of columns and rows, respectively, under control of CPU (see Figs. 3-5; col. 4, lines 35-67).

Regarding claim 10, the signal processing circuit (32) includes a video outputting (112, 36) for feeding a processed signal to the display (see Figs. 1A & B; col. 6, lines 6-23).

Regarding claim 11, the claimed limitations are analyzed with respect to claim 1.

Regarding claim 15, the claimed limitations are analyzed with respect to claim 5.

Regarding claim 16, the claimed limitations are analyzed with respect to claim 6.

Regarding claim 17, the claimed limitations are analyzed with respect to claim 7.

Regarding claim 18, the claimed limitations are analyzed with respect to claim 10.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 – 4 & 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 6,529,236) in view of Takahashi (JP 06-141330).

Regarding claim 2, Watanabe discloses the processing circuit (28) further clamps image signal at preselected level, and subjects the claimed image signal to white balance adjustment, color correction, tonality correction, and so forth. Watanabe does not expressly teach a color

Art Unit: 2615

separating circuit for separating a signal output via color filters included in the image pickup section color by color; a frequency band limiting circuit for limiting a frequency band of each output of the color separating circuit; and multiplexing circuit for multiplexing outputs of the frequency band limiting circuit; wherein the color separating circuit, the frequency band limiting circuit and the multiplexing circuit are arranged between the noise reducing circuit and the digitizing circuit. However, as taught by Takahishi, a color separating circuit for separating color signal output from CDS circuit into each color signal R, G and B, and each color signal is inputted to low pass filters (5-7), in which the signal is amplified and only a valid signal of video signal band is extracted with the filter having a lower cut-off frequency than the frequency of a half of the sampling frequency, and further the resulting signal is synthesized/multiplexed into a serial signal by circuit (11) for reducing distortion attended with sampling process at A/D conversion (see Abstract & Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art to modify Watanabe with Takahishi by including a color separating circuit, frequency band limiting circuit and multiplexing circuit to be arranged between the noise reducing circuit and A/D converter for reducing reflection distortion attended with sampling at A/D conversion so that picture deterioration is prevented.

Regarding claim 3, Takahashi discloses that the low pass filters (5-7) in which only valid signal of the video signal band is extracted with the filter having a lower cut-off frequency than the frequency of a half of the sampling frequency (see Constitution).



Art Unit: 2615

Regarding claim 4, Takahishi also discloses an analog adding circuit (11) for adding (synthesizing) the resulting color signal output from each low pass filter corresponding to a particular color as shown in Fig. 2 & Constitution.

Regarding claim 12, the claimed limitations are analyzed with respect to claim 2.

Regarding claim 13, the claimed limitations are analyzed with respect to claim 3.

Regarding claim 14, the claimed limitations are analyzed with respect to claim 4.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 6,529,236) in view of Watanabe (US 6,522,356).

Regarding claim 9, Watanabe '236 does not teach that the photosensitive devices have geometric centers shifted from each other by a distance corresponding to one half of a pitch of the plurality of photosensitive devices in a direction of rows. However, as taught by Watanabe '356, it is a well-known configuration for an image pickup section to have the pixels disposed in even-number rows being shifted by one half of a pitch in direction of rows from corresponding pixels disposed in odd-number rows to obtain a well-balanced color resolution of the image pickup section (see Figs. col. 3, lines 21-26; col. 4, lines 44-45).

Therefore, it would have been obvious to one of ordinary skill in the art to modify Watanabe '236 with Watanabe '356 by reconfiguring the image pickup section in a well-known

Art Unit: 2615

fashion in which nearby ones of the plurality of photosensitive devices have geometric shifted from each other by a distance corresponding to one half of a pitch of the plurality of photosensitive devices in a direction of rows to obtain a well-balanced color resolution of the image pickup section.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

NT.  
July 18, 2003



ANDREW CHRISTENSEN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600